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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,359	01/21/2004	Yoshihiro Saeki	030712-21	8709

22204 7590 06/16/2005

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EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,359	SAEKI ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Goto (US 2004/0018661.)

In regard to claims 1 and 2, in figs. 1 and 3, Goto discloses a semiconductor device 400 comprising:

a first semiconductor chip 403;

a second semiconductor chip 405 which is mounted on the first semiconductor chip (fig.1);

a first electrode group 407A which is formed on the first semiconductor chip and arranged along an outer periphery of the first semiconductor chip in such a manner as to surround the second semiconductor chip (fig. 3);

a second electrode group 407B which is formed on the first semiconductor chip and arranged along the outer periphery of the first semiconductor chip in such a manner as to surround the first electrode group (fig. 1);

a third electrode 406 group which is formed on the second semiconductor chip (fig. 3);

a plurality of first wires 409 for electrically connecting the first electrode group and the third electrode group to each other; and

external connection terminals (on the element 402) which are electrically connected to the second electrode group,

wherein the first semiconductor chip comprises a first circuit element region which is surrounded by the first electrode group, and a second circuit element region which surrounds the first electrode group and is surrounded by the second electrode group. It should be noted that the connection groups are formed on the active of the chip 403. This active surface contains or composes a plurality of devices; therefore, the circuit elements are surrounded by the connection groups.

In regard to claim 3, Goto further discloses the external connection terminals are conductive leads, leads 402 (section [0018]);

the plurality of leads are arranged along the outer periphery of the first semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance (fig. 3); and

the second electrode group and the leads are electrically connected to each other by a plurality of second wires 110 (fig. 3).

In regard to claim 4, Goto further discloses that the size of the second semiconductor chip is smaller than that of the first semiconductor chip (fig. 3.)

In regard to claim 5, Goto further discloses that the first semiconductor chip and the second semiconductor chip are sealed with a resin108 (fig. 1.)

In regard to claim 6, Goto further discloses the external connection terminals are conductive leads (as addressed in claim 3 above);

the plurality of leads are arranged along the outer periphery of the first semiconductor chip at positions separate from the first semiconductor chip by a predetermined distance;

the second electrode group and the leads are electrically connected to each other by a plurality of second wires (fig.1);

the first semiconductor chip and the second semiconductor chip are sealed with a resin; and

the first wires and the second wires are sealed with the resin (see also the above discussions regarding to claims 1-3.

In regard to claim 7, Goto further discloses that the first semiconductor chip is formed on a support 101 (fig. 1.)

8. The semiconductor device according to claim 1,as mentioned above the first electrode group and the second electrode group are formed along sides of the outer periphery of the first semiconductor device (see claim 1, for example.)

In regard to claim 9, Goto further discloses the third electrode group is formed along an outer periphery of the second semiconductor chip (fig. 3.)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
June 12, 2005